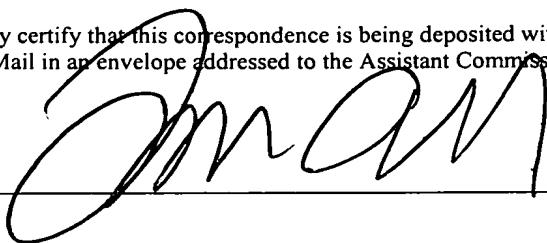


Docket No.: GR 99 P 1058

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on the date indicated below.

By: 

Date: January 22, 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Wilfried Daehn  
RCE of  
Applic. No. : 09/484,781, filed January 18, 2000  
RCE filed : January 22, 2002  
Title : Integrated Semiconductor Circuit and Method for Functional Testing of Pad Cells  
Examiner : Don P. Le - Art Unit: 2819

#10  
J. Lang  
3/14/02

INFORMATION DISCLOSURE STATEMENT  
UNDER 37 C.F.R. 1.98

Hon. Commissioner of Patents and Trademarks,  
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 5,471,153 (Martin), dated November 28, 1995;

U.S. Patent No. 5,559,441 (Desroches), dated September 24, 1996;

U.S. Patent No. 5,621,740 (Kamada), dated April 15, 1997;

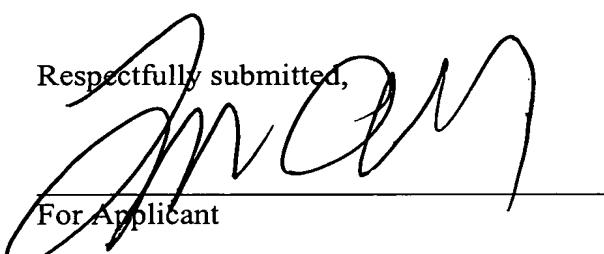
Published, European Patent Application No. EP 0 855 662 A1 (Bonitz), dated July 29, 1998.

European Search Report, dated June 5, 2001.

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If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

  
For Applicant

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Date: January 22, 2002

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